REMARKS

Claims 1-15 and 24-27 were pending in the Application. Claim 1 is an independent claim and claims 2-9 depend there from. Claim 10 is an independent claim and claims 11-12 depend there from. Claim 13 is an independent claim and claims 14-15 depend there from. Claim 24 is an independent claim and claims 25-27 depend there from. Claims 1, 10, 13 and 26 are currently amended. Applicant respectfully requests reconsideration of the application in light of the above amendments and the following remarks.

Rejections Under 35 U.S.C. §102(b) and 103(a)

Claims 1-15 and 25-27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Goldberg (U.S. Patent No. 6,874,062) in view of Lehman (U.S. Patent No. 6,658,437). Further, claim 24 was rejected under 35 U.S.C. §102(b) as being anticipated by Goldberg. The Applicant respectfully traverses the above-mentioned rejections for at least the following reasons.

Regarding claim 1, Applicant respectfully submits that the proposed combination of references fails to teach, suggest, or disclose at least, for example, "a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when the first memory block has a memory segment that is available for data storage and a second state when the first memory block does not have a memory segment that is available for data storage, wherein the first state comprises at least a portion of a memory address of the first memory block," as set forth in Applicant's amended, independent claim 1.

The Applicant appreciates the Examiner's recognition that "Goldberd [sic] does not explicitly disclose the details of having the first state include at least a portion of a memory address of the first memory block." (Office Action, Page 5, Lines 20-21). However, the Applicant disagrees with the Office Action's characterization that "Lehman discloses having the

first state includes at least a portion of a memory address of the first memory block." (Office Action, Page 6, Lines 1-2). The "First Point of Argument" Section of the final Office Action states that "Lehman discloses 'a first state of a logic circuit associated with the first memory block comprising at least a portion of the memory address of the first memory block;' because Applicant's specification clearly describes determining address portions of memory segments based on the position of the identified block flag (Description of Figure 3) which is clearly disclosed by Lehman (See above)." (Office Action, Point 24, Pages 19-20). However, "determining address portions of memory segments based on the position of the identified block flag" is different than "the first state comprises at least a portion of a memory address of the first memory block," as set forth in Applicant's independent claim 1. Applicant's specification sets forth several embodiments. For example, with regard to the memory address, Applicant's specification states the following:

> The address-determining step 1040 determines an address of the available memory segment corresponding to the previously-identified segment flag and optionally, the previously-identified block flag. **The address-determining step 1040 may be accomplished in a variety of ways. For example, various information may be contained in the segment or block flags that the step 1040 may utilize to calculate the segment address.** *Alternatively, for example, the step 1040 may convert the position of the identified segment flag in the set of segment flags to the address of the memory segment. Alternatively, for example, the step 1040 may also utilize the position of the identified block flag in the set of block flags to determine a portion of the available memory segment's address.*

(Applicant's Specification, Page 29, Paragraph [96], Lines 3-11 (emphasis added)). As shown above, Applicant's specification distinguishes between "determining address portions of memory segments based on the position of the identified block flag" and "the first state comprises at least a portion of a memory address of the first memory block," as set forth in Applicant's independent claim 1. Thus, even if Lehman does disclose determining address portion of memory segments based on the position of the identified block flag, that is different than "the first state comprises at least a portion of a memory address of the first memory block." Nowhere in the combination of Goldberg and Lehman is there any disclosure of "the first state comprises at least a portion of a

memory address of the first memory block," as set forth in Applicant's independent claim 1. The cited sections of Lehman in the final Office Action (e.g., Col. 10, line 50-Col. 11, line 15; Col. 11, lines 38-46; Figure 7 and related text; Figure 9 and related text), all discuss assigning an address to a bit based on the position of the bit. A bit position being associated with an address is different than "**the first state comprises** at least a portion of a memory address." Because the combination of Goldberg in view of Lehman fails to teach or suggest all the claim limitations, a rejection under 35 U.S.C. §103(a) cannot be maintained.

Additionally, as discussed above, Goldberg teaches away from combination with Lehman. In Column 2, Lines 11-44, Goldberg discusses the disadvantages of using a multiple buffer pool implementation as described in Lehman. For example, Goldberg states that "[t]he use of multiple buffer pools allows storage resources to be allocated in a manner that conserves system resources. However, depending on the number of pools created within the system, more memory may still be allocated than is necessary." (Goldberg, Column 2, Lines 28-30). Additionally, Goldberg goes on to teach away from Lehman by stating the following:

> Another disadvantage associated with the foregoing buffer pool mechanisms involves the amount of storage space consumed by the data structures such as linked lists that are required to implement the buffer pools. Each entry in a linked list must include both an address pointer to the associated buffer, and must also contain at least one address pointer to another entry in the list. If the list is a doubly-linked list, two such address pointers to the linked entries are needed. Therefore, as the number of buffers in the data pool increases, the size of the linked list becomes prohibitive.

(Goldberg, Column 2, Lines 35-44). Further, Goldberg teaches away from using multiple bits representations (Goldberg, Column 3, Lines 5-9) as disclosed in Lehman (Lehman, Column 11, Lines 47-57). Goldberg specifically touts the advantages of single bit representation. For example, Goldberg states that "since only a single bit is required to describe whether each section of storage is allocated, a much smaller amount of memory is associated with the use of bitmaps as compared to the use of linked lists." (Goldberg, Column 3, Lines 5-9). The final Office Action repeatedly states that the motivation to combine the references is because

"Lehman discloses ['a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions' (Col. 2, lines 42-48]." However, despite Lehman's efforts to make multiple buffer pool implementations require less space to store allocation information, Goldberg teaches staying away from multiple buffer pool implementations altogether. Clearly, there is no motivation to combine Goldberg and Lehman. Rather, Goldberg teaches away from combining with Lehman. Because Goldberg cannot be combined with Lehman, the rejection under 35 U.S.C. §103(a) cannot be maintained.

Regarding claim 10, Applicant respectfully submits that the proposed combination of references fails to teach, suggest, or disclose at least, for example, "a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when the first memory block has a memory segment that is available for data storage and a second state when the first memory block does not have a memory segment that is available for data storage; wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block," as set forth in Applicant's amended, independent claim 10.

Applicant has amended independent claim 10 to recite "wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block." Applicant's amendment is supported by the Applicant's specification (e.g., Applicant's Specification, Page 10, Paragraph [34]). Clearly, the combination of Goldberg and Lehman fails to disclose "wherein **the first state of the first logic circuit comprises a number of available memory segments** in the first memory block," as set forth in Applicant's amended, independent claim 10. Rather, Lehman teaches looking at an entire bit map to count up the number "0" bits in the bit map. As stated in Lehman, "logical groups inside the 16 bits must be determined **by examining adjacent bits**." (Lehman, Column 11, Lines 8-9). Thus, Lehman does not teach "**the first state of the first logic circuit comprises a number of available memory segments in the first memory block**" wherein the "first logic circuit [is] associated **exclusively** with [the] first

memory block." Further, the Applicant appreciates the Examiner's recognition that "Goldberd [sic] does not expressly disclose the details of wherein the first state of the first logic circuit comprises information indicating a number of available memory segments in the first memory block." (Office Action, Page 13, Lines 19-21). Because the combination of Goldberg in view of Lehman fails to teach or suggest all the claim limitations, a rejection under 35 U.S.C. §103(a) cannot be maintained.

Additionally, as discussed above, Goldberg teaches away from combination with Lehman. In Column 2, Lines 11-44, Goldberg discusses the disadvantages of using a multiple buffer pool implementation as described in Lehman. For example, Goldberg states that "[t]he use of multiple buffer pools allows storage resources to be allocated in a manner that conserves system resources. However, depending on the number of pools created within the system, more memory may still be allocated than is necessary." (Goldberg, Column 2, Lines 28-30). Additionally, Goldberg goes on to teach away from Lehman by stating the following:

> Another disadvantage associated with the foregoing buffer pool mechanisms involves the amount of storage space consumed by the data structures such as linked lists that are required to implement the buffer pools. Each entry in a linked list must include both an address pointer to the associated buffer, and must also contain at least one address pointer to another entry in the list. If the list is a doubly-linked list, two such address pointers to the linked entries are needed. Therefore, as the number of buffers in the data pool increases, the size of the linked list becomes prohibitive.

(Goldberg, Column 2, Lines 35-44). Further, Goldberg teaches away from using multiple bits representations (Goldberg, Column 3, Lines 5-9) as disclosed in Lehman (Lehman, Column 11, Lines 47-57). Goldberg specifically touts the advantages of single bit representation. For example, Goldberg states that "since only a single bit is required to describe whether each section of storage is allocated, a much smaller amount of memory is associated with the use of bitmaps as compared to the use of linked lists." (Goldberg, Column 3, Lines 5-9). The final Office Action repeatedly states that the motivation to combine the references is because "Lehman discloses ['a data space management system that requires less space to store allocation

information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions' (Col. 2, lines 42-48]." However, despite Lehman's efforts to make multiple buffer pool implementations require less space to store allocation information, Goldberg teaches staying away from multiple buffer pool implementations altogether. Clearly, there is no motivation to combine Goldberg and Lehman. Rather, Goldberg teaches away from combining with Lehman. Because Goldberg cannot be combined with Lehman, the rejection under 35 U.S.C. §103(a) cannot be maintained.

Regarding claim 13, Applicant respectfully submits that the proposed combination of references fails to teach, suggest, or disclose at least, for example, "a first logic circuit associated exclusively with a first memory block of the plurality of memory blocks, the first logic circuit having a first state when the first memory block has a memory segment that is available for data storage and a second state when the first memory block does not have a memory segment that is available for data storage; wherein the second state of the first logic circuit comprises information indicating an offset to available memory," as set forth in Applicant's amended, independent claim 13.

The Applicant appreciates the Examiner's recognition that "Goldberg...doesn't expressly disclose the second state of the first logic circuit comprise information indicating an offset to available memory." (Office Action, Page 16, Lines 14-17). However, the Applicant disagrees with the Office Action's characterization that "Lehman discloses the second state of the first logic circuit comprise information indicating an offset to available memory." (Office Action, Page 6, Lines 1-2). The final Office Action cites various section of Lehman (e.g., Col. 9, lines 53-60; Col. 10, lines 1-10; Figure 7 and related text); however, the cited sections of Lehman discuss using count arrays and pointer arrays to search for free blocks. By using pointers to identify free blocks, Lehman teaches away from "a first logic circuit associated **exclusively** with a first memory block...wherein the second state of the first logic circuit comprises information indicating an offset to available memory," as set forth in Applicant's amended, independent claim 13. Because the combination of Goldberg in view of Lehman fails to teach or suggest all the

claim limitations, a rejection under 35 U.S.C. §103(a) cannot be maintained.

Additionally, as discussed above, Goldberg teaches away from combination with Lehman. In Column 2, Lines 11-44, Goldberg discusses the disadvantages of using a multiple buffer pool implementation as described in Lehman. For example, Goldberg states that "[t]he use of multiple buffer pools allows storage resources to be allocated in a manner that conserves system resources. However, depending on the number of pools created within the system, more memory may still be allocated than is necessary." (Goldberg, Column 2, Lines 28-30). Additionally, Goldberg goes on to teach away from Lehman by stating the following:

> Another disadvantage associated with the foregoing buffer pool mechanisms involves the amount of storage space consumed by the data structures such as linked lists that are required to implement the buffer pools. Each entry in a linked list must include both an address pointer to the associated buffer, and must also contain at least one address pointer to another entry in the list. If the list is a doubly-linked list, two such address pointers to the linked entries are needed. Therefore, as the number of buffers in the data pool increases, the size of the linked list becomes prohibitive.

(Goldberg, Column 2, Lines 35-44). Further, Goldberg teaches away from using multiple bits representations (Goldberg, Column 3, Lines 5-9) as disclosed in Lehman (Lehman, Column 11, Lines 47-57). Goldberg specifically touts the advantages of single bit representation. For example, Goldberg states that "since only a single bit is required to describe whether each section of storage is allocated, a much smaller amount of memory is associated with the use of bitmaps as compared to the use of linked lists." (Goldberg, Column 3, Lines 5-9). The final Office Action repeatedly states that the motivation to combine the references is because "Lehman discloses ['a data space management system that requires less space to store allocation information in order to increase the speed of disk access operations in allocating, storing, and retrieving data values, and also to free up space for use in other control functions' (Col. 2, lines 42-48]." However, despite Lehman's efforts to make multiple buffer pool implementations require less space to store allocation information, Goldberg teaches staying away from multiple buffer pool implementations altogether. Clearly, there is no motivation to combine Goldberg

and Lehman. Rather, Goldberg teaches away from combining with Lehman. Because Goldberg cannot be combined with Lehman, the rejection under 35 U.S.C. §103(a) cannot be maintained.

The Applicant respectfully submits that, based upon the above, the proposed combination of Goldberg in view of Lehman fails to teach or suggest by themselves or in combination all of the limitations of Applicant's independent claims 1, 10 and 13, and that the rejections of claims 1, 10 and 13 under 35 U.S.C. §103(a) cannot be maintained. Therefore, Applicant respectfully requests that the rejections of claims 1, 10 and 13 under 35 U.S.C. §103(a), be withdrawn.

Because dependent claims 2-9, 11-12 and 14-15 depend, directly or indirectly, from independent claim 1, 10 or 13, and because claims 1, 10 and 13 are allowable over the proposed combination of references, the Applicant asserts that rejections of dependent claims 2-9, 11-12 and 14-15 are now moot. The Applicant asserts that claims 2-9, 11-12 and 14-15 are also allowable over the proposed combination of references and requests that the rejections of claims 1-15 under 35 U.S.C. §103(a), be withdrawn.

Regarding claims 24-27, for reasons similar to those stated previously, the Applicant submits that such claims are allowable.

For example and without limitation, for reasons generally analogous to those stated previously with regard to claim 1, the Applicant submits that claim 25 is allowable over Goldberg, and over Goldberg in view of Lehman.

Also for example, for reasons generally analogous to those stated previously with regard to claim 10, the Applicant submits that claim 26 is allowable over Goldberg, and over Goldberg in view of Lehman.

Further for example, for reasons generally analogous to those stated previously with regard to claim 13, the Applicant submits that claim 27 is allowable over Goldberg, and over Goldberg in view of Lehman.

The Office Action makes various statements regarding former claims 1-15 and 24-27, 35 U.S.C. § 102(b), 35 U.S.C. § 103(a), the Goldberg reference, the Lehman reference, one of skill in the art, etc. that are now moot in view of the above-mentioned amendments and/or arguments. Thus, the Applicants will not address all of such statements at the present time. However, the Applicants expressly reserve the right to challenge such statements in the future should the need arise (e.g., if such statements should become relevant by appearing in a rejection of any current or future claim).

Applicant reserves the right to argue additional reasons supporting the allowability of claims 1-15 and 24-27 should the need arise in the future.

CONCLUSION

Applicant respectfully submits that claims 1-15 and 24-27 are in condition for allowance, and requests that the application be passed to issue.

Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Date: March 17, 2008

Respectfully submitted,

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